**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**
**PATENT APPLICATION**

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| Application No. | : | 10/748,023 | Confirmation No.: 6463 |
| Applicants | : | Muthiah Venkateswaran | |
| Filed | : | December 30, 2003 | |
| TC/A.U. | : | 2826 | |
| Examiner | : | Andujar, Leonardo | |
| Docket No. | : | TI-36587 | |
| Customer No. | : | 23494 | |

**COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE**

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Dear Sir;

Responsive to the Office action of March 13, 2006, NOTICE OF ALLOWANCE AND FEE(S) DUE, applicant respectfully makes the following comments on the statement of reasons for allowance:

**Comments on the statement of reasons for allowance:**

Applicant thanks Examiner Andujar for his careful examination of this application and the allowance of claims 1-10 and 20. In response to the statement of reasons for allowance, applicant respectfully submits that the reason set forth in the Notice of Allowance includes limitation not in the allowed claims:

Claims 1 and 20 are copied as follows:

Claim 1

A method of forming an underfilled chip package, comprising:

depositing a underfill material over a surface of a package substrate to form an underfill region;

placing a die having a plurality of solder bumps at an angle relative to the package substrate such that one or more of the solder bumps adjacent a first side of the die contact the surface of the package substrate within the underfill region while one or more of the solder bumps adjacent a second side of the die opposite the first side of the die are generally located at a distance away from the surface of the package substrate; and

moving the second side of the die toward the surface of the package substrate until the one or more solder bumps adjacent the second side of the die contact the surface such that the underfill material is forced into the area between the plurality of bumps.

Claim 20

A method of forming an underfilled chip package, comprising:

depositing a underfill material over a surface of a package substrate to form an underfill region;

placing a die having a plurality of solder bumps at an angle relative to the package substrate such that one or more of the solder bumps adjacent a first

side of the die contact the surface of the package substrate within the underfill region while one or more of the solder bumps adjacent a second side of the die opposite the first side of the die are generally located at a distance away from the surface of the package substrate; and

moving the second side of the die toward the surface of the package substrate by rotating the die about the points of contact between the one or more solder bumps adjacent the first side of the die and the surface of the package substrate until the one or more solder bumps adjacent the second side of the die contact the surface, wherein such rotation of the die causes at least a portion of the underfill material to flow generally in a direction from the first side of the die toward the second side of the die and into the area between the plurality of bumps; and

performing a heated reflow process to connect the solder bumps to the surface of the packing substrate and to cure the underfill material.

Applicant respectfully submits that claims 1 and 20 do not include a limitation of forming an under filled chip package where a bumped chip is diagonally attached.

Respectfully submitted,

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